

Power Macintosh 7200/8200 speedup

The Power Macintoshes 7200/8200 have a clock generator built with a MPC 956 - Motorola PLL clock driver. The MPC 956 have four sense pins (S0..S3) allows to set one of 14 possible configurations (0..13). These configurations sets the speed factors for the CPU and bus clock.

No	S3	S2	S1	S0	CPU clock factor	Bus clock factor
0	0	0	0	0	2.0	1.0
1	0	0	0	1	2.4	1.2
2	0	0	1	0	2.4	0.8
3	0	0	1	1	3.03	1.5
4	0	1	0	0	3.03	1.0
5	0	1	0	1	3.6	1.8
6	0	1	1	0	3.6	1.2
7	0	1	1	1	3.6	0.9
8	1	0	0	0	4.0	2.0
9	1	0	0	1	4.0	1.3
10	1	0	1	0	4.0	1.0
11	1	0	1	1	4.5	2.3
12	1	1	0	0	4.5	1.5
13	1	1	0	1	4.5	1.12
14	1	1	1	0	not used	not used
15	1	1	1	1	not used	not used

The 7200/90 have a 20MHz crystal and uses the configuration 11. So we have:

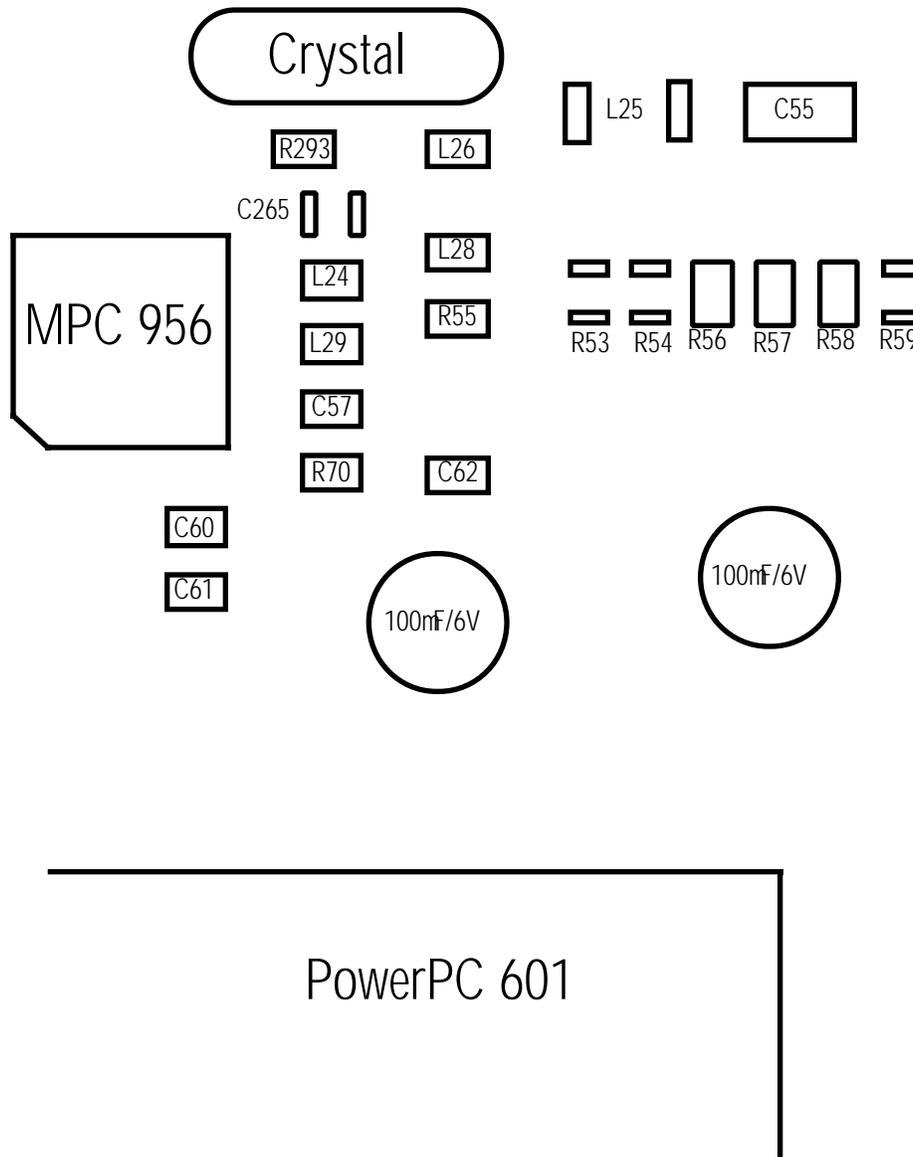
- CPU clock: $20\text{MHz} \times 4.5 = 90\text{ MHz}$
- Bus clock: $20\text{MHz} \times 2.3 = 46\text{ MHz}$

The configuraion settings are made by 8 resistors on the bord nearly CPU and the MPC956.

	0		1	
S0	R53=100	R70 not used	R70=10k	R53 not used
S1	R54=100	R56 not used	R56=10k	R54 not used
S2	R58=100	R57 not used	R57=10k	R58 not used
S3	R59=100	R55 not used	R55=10k	R59 not used

The configuration 11 means:

- S0=1: R70=10kOhm and R53 is not soldered
- S1=1: R56=10kOhm and R54 is not soldered
- S2=0: R58=100Ohm and R57 is not soldered
- S3=1: R59=10kOhm and R55 is not soldered



Layout of a 7200/90 Board

Warning!

To modificate the clock you need 100 Ohm and 10kOhm 0805 type SMD resistors, perharps an crystal if you want to change them too and some electronic stuff like a temperature-regulated soldering station. If you are not familiar with electronics, ask a friend who knows it. In other case you can damage your Mac! And off course there is no guarantee...

My 7200/90 worked with a 33MHz crystal and configuration 3 at 100MHz CPU and 50MHz bus clock, but I got after 3 hours running some vertical lines on the screen only when I rebooted my Mac. My machine works now at 100MHz CPU and 33MHz bus speed. 120MHz was not possible on my 7200...

Peter